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INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

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ENG, DAVID Y	

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heather.l.adamson@intel.com
docketing@cpaglobal.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GILBERT WOLRICH, DEBRA BERNSTEIN, MATTHEW J. ADILETTA and DONALD F. HOOPER

Appeal 2009-006790
Application 09/475,614[1]
Technology Center 2400

Before LANCE LEONARD BARRY, CAROLYN D. THOMAS, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

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[1] Application filed December 30, 1999. The real party in interest is Intel Corporation.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's final decision rejecting claims 1-25 and 44, which are all the claims under review in the application, as claims 26-43 withdrawn non-elected claims. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We AFFIRM.

The present invention is directed towards receiving data from a network and issuing a receive request directing the transfer of data from one of the plurality of device ports to a buffer memory and specifying a thread from among a plurality of processing threads to process the data. (Spec., 1, l. 23 to 2, l. 4.)

Claim 1 is illustrative:

> 1. A method of receiving data from a network, comprising:
>
> issuing a request directing a transfer of data from one of a plurality of device ports to a storage unit and specifying a thread from among a plurality of processing program threads to process the data.

Appellants appeal the following rejection:

Claims 1-25 and 44 under 35 U.S.C. § 103(a) as unpatentable over Allison (US 6,373,848 B1, Apr. 16, 2002) and Belkin (US 6,604,125 B1, Aug. 5, 2003).

FACTUAL FINDINGS

Allison

1a. Allison discloses that in one prior art embodiment, "multiple copies of a single MAC [Media Access Control Unit] design are replicated in a VSLI chip to serve the respective ports." (Col. 1, ll. 31-33.)

1b. In Allison, "[t]he single MAC reduces the circuit count for the adapter as compared to prior art devices using multiple MACs for transferring data." (Col. 12, ll. 5-8.)

1c. Allison discloses that "[t]he transmit and receive state machines operate concurrently and determine the MAC state for servicing the port." (Col. 3, ll. 2-4.)

Belkin

2a. Belkin discloses a mechanism for servicing requests in a multi-threaded system. (Col. 2, l. 66 to col. 3, l. 1.)

2b. In Belkin, "[w]hen a request is received, it is processed to determine with which thread pool the request is to be associated." (Col. 3, ll. 21-23.)

ANALYSIS

In essence, Appellants argue claims 1-25 and 44 as a group (App. Br. 9-17). For claims 2-25 and 44, Appellants repeat the same argument made for claim 1. We will, therefore, treat claims 2-25 and 44 as standing or falling with claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

Issue1: Did the Examiner err in finding that the combination of Allison and Belkin discloses issuing a request specifying a thread from among a plurality of processing program threads to process the data, as set forth in claim 1?

Appellants contend that "Allison does not describe a system with multiple program threads[,] [t]hus, Allison does not describe a request specifying a particular one from multiple program threads." (App. Br. 14.)

The Examiner found that "[t]he request as recited [in claim 1] is actually a command instructing the system to transfer data from one of a plurality of ports to a buffer memory." (Ans. 8.) The Examiner further found that "Allison teaches a plurality of groups of instructions for processing the data depending on the state of the machine. If the groups of instructions are organized in a multithread environment as taught by Belkin, a thread would be selected from among a plurality of threads for processing the data so that the system would run more efficiently." (Ans. 9.) We agree with the Examiner.

Here, Appellants primarily direct their arguments towards Allison and contend that Allison does not disclose a request that specifies a thread from a plurality of threads. (*see* App. Br. 11-14.) However, we point out that it is the combination of Allison and Belkin that the Examiner is relying on to teach the above-noted limitations.

Specifically, Allison discloses a multi-port adapter having a Media Access Control (MAC) chip for transferring data between a host system and a TDM communication system and that control logic is coupled to the storage register to control the transfer of data between the system and the

storage registers. (Allison, *see* Abstract.) Allison also discloses that prior art systems used multiple MAC designs for transferring data (FF 1a -1b). In other words, Allison discloses both a single MAC serving all ports and multiple MACs serving respective ports. We find that the multiple MACs embodiment described in Allison suggests the use of multiple control/processing units to transfer data from a plurality of ports to a storage unit. We further find that having multiple control units working concurrently necessarily requires specifying a particular control unit to process specific data, given that there is a plurality of control units. While Allison's multiple MAC design results in a large number of gates (a high cost for the chip) (Allison, Col. 1, ll. 34-35), such a design still shows that it was known at the time of the invention to use multiple control/processing units, i.e., multiple threads. Like the MACs in Allison, a "thread" is a unit of processing scheduled by an operating system. Thus, we find that Allison's *multiple MACs* embodiment act as *multiple threads* as each MAC concurrently processes data.

The Examiner similarly found that Allison's transmit interface (TxMll) and receive interface (RxMII) select one of a plurality of threads (i.e., TxMAC or RxMAC) to process data in a single MAC embodiment (Ans. 5; *see* also Fig. 1). As for Allison's single MAC embodiment, such an embodiment discloses using multiple threads in that a transmit MAC (TxMAC) and a receive MAC (RxMAC) are contained within the single MAC (*see* Allison's Fig. 1). In Allison, the transmit and receive state machines operate concurrently and determine the MAC state (FF 1c). This functionality of Allison clearly suggests a multi-thread environment given the concurrent processing. Also, Allison must necessarily specify which

processing unit to use, e.g. TxMAC or RxMAC, depending on the type of operation being performed.

To summarize, for reasons set forth above, we find that Allison discloses issuing a request directing a transfer data from a plurality of ports and specifying a thread to process the data. In addition, the Examiner found that Belkin discloses a mechanism for servicing requests in a multi-threaded system (FF 2a). For example, in Belkin, when a request is received, it is processed to determine which thread to use (FF 2b). Therefore, we find that both Allison and Belkin disclose a multi-thread environment and Allison discloses issuing a request to transfer data. As such, based upon our review of the record, we find that the weight of the evidence supports the Examiner's position as articulated in the Answer.

The test for obviousness is what the combined teachings of the references would have suggested to the artisan. Accordingly, one can not show nonobviousness by attacking references individually where the rejection is based on a combination of references. *In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Here, we find that the combination of Allison and Belkin teaches or suggests the features noted *supra*.

Therefore, for at least the reasons set forth above, we find that the combination of Allison and Belkin teaches or suggests the claimed invention as set forth in claim 1.

Issue2: Did the Examiner err in combining Allison and Belin?

Appellants "disagree that one skill[ed] in the art would be motivated to provide the threads of Belkin in the adapter of Allison." (App. Br. 15.) Appellants further contend that "the motivation to move the high level [] OS

supported threads from a processor 604 of Belkin to a low level MAC adapter is contrary to Allison's stated goal of reducing gate count." (App. Br. 15-16.) We disagree.

The Supreme Court has held that in analyzing the obviousness of combining elements, a court need not find specific teachings, but rather may consider "the background knowledge possessed by a person having ordinary skill in the art" and "the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-41 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions," and the basis for an obviousness rejection must include an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*

Here, the Examiner has found actual teachings in the prior art and has provided a rationale for the combination (*see* Ans. 6-7). Further, the teachings suggest that the combination involves the predictable use of prior art elements according to their established functions. For example, concurrent processing as taught in both Allison and Belkin clearly suggest using a plurality of threads and having the capability to select therefrom. Accordingly, we find that the Examiner has provided sufficient motivation for modifying Allison with the teachings of Belkin, and we will sustain the obviousness rejection of claims 1-25 and 44.

As a final note, our records reflect that Appellants' petition under 37 CFR 1.183, filed June 19, 2008, requesting a waiver of 37 CFR 41.41(1)(2) which sets forth a two month period for filing a Reply Brief, was dismissed. As such, Appellants' untimely Reply Brief will not be considered.

In view of the above discussion, since Appellants have not demonstrated that the Examiner erred in finding the argued limitations in the disclosure of Allison and Belkin, the Examiner's 35 U.S.C. § 103(a) rejection of representative independent claim 1, as well as claims 2-25 and 44 not separately argued by Appellants, is sustained.

DECISION

We affirm the Examiner's § 103 rejections.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2010).

AFFIRMED

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INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402